In the Claims

1. (Currently Amended) An active pixel sensor circuit comprising:

a photodetector;

a reset transistor connected between the photodetector and a first bus;

a snapshot transistor having a node connected to the photodetector;

a driver transistor connected to a ~~second~~ row driver bus and the snapshot transistor; and

an isolation transistor connected between the driver transistor and a column bus;

wherein the transistors are MOSFETs and a tapered reset signal is applied to the reset transistor in order to reset the photodetector.

2. Cancelled

3. Cancelled

4. (Previously Presented) The active pixel sensor circuit of Claim 1, wherein a charge from the photodetector is transferred to a gate capacitance of the driver transistor via the snapshot transistor.

5. (Original) The active pixel sensor circuit of Claim 4, wherein the reset transistor discharges any charge left on the photodetector along with any charge on the gate of the driver transistor during a reset operation.

6. (Original) The active pixel sensor circuit of Claim 5, wherein the reset transistor is disabled during a signal integration mode and a snapshot image capture mode.

7. (Original) The active pixel sensor circuit of Claim 6, wherein, after snapshot image capture, the reset transistor is enabled in order to drain any unwanted charge that is generated after the integration mode.

8. (Original) The active pixel sensor circuit of Claim 7, further comprising a column buffer connected to the column bus.

9. (Currently Amended) The active pixel sensor circuit of Claim 8, further comprising a row driver circuit connected to the driver transistor via the row driver bus.

10. (Previously Presented) An active pixel sensor circuit comprising:

photodetector means for converting light into an electrical signal;

image snapshot means connected to the photodetector for transferring the signal from the photodetector;

reset means for resetting the photodetector after the image has been transferred;

amplifier means for amplifying the signal from the snapshot means; and

isolation means for isolating the circuit from a column bus;

wherein a tapered reset signal is applied to the reset means in order to reset the photodetector means.

11. Cancelled

12. Cancelled

13. Cancelled

14. (Currently Amended) A CMOS imager array comprising a plurality of pixels, each pixel comprising:

a photodetector;

a reset MOSFET having a source connected to the photodetector, a gate connected to a reset input signal, and a drain connected to a first bus;

a snapshot MOSFET having a source connected to the photodetector and a gate connected to a snapshot signal;

a driver MOSFET having a drain connected to a ~~second~~ row driver bus and a gate connected to a drain of the snapshot MOSFET; and

an isolation MOSFET having a drain connected to a source of the driver MOSFET, a gate connected to an access signal, and a source connected to a column bus;

wherein a tapered reset signal is applied to the reset MOSFET in order to reset the photodetector.

15. (Original) The imager array of Claim 14, wherein the reset, snapshot, driver and isolation MOSFETs are all of the same polarity.

16. (Currently Amended) The imager array of Claim 15, further comprising a row driver circuit connected to the ~~second~~ row driver bus.

17. (Original) The imager array of Claim 16, further comprising a column buffer circuit connected to the column bus.

18. Cancelled

19. (New) An active pixel sensor circuit comprising:

a photodetector;

a reset transistor connected between the photodetector and a first bus;

a snapshot transistor having a node connected to the photodetector;

a driver transistor connected to a row driver bus and the snapshot transistor;

a row driver circuit connected to the row driver bus;

an isolation transistor connected between the driver transistor and a column bus; and

a column buffer connected to the column bus;

wherein the transistors are MOSFETs and a tapered reset signal is applied to the reset transistor in order to reset the photodetector, and wherein during a reset operation, the row driver circuit grounds the driver transistor such that at least a portion of the column buffer acts as a current source for a feedback amplifier formed by the driver transistor, isolation transistor, and the column buffer.

20. (New) A CMOS imager array circuit comprising:

a photodetector;

a reset MOSFET having a source connected to the photodetector, a gate connected to a reset input signal, and a drain connected to a first bus;

a snapshot MOSFET having a source connected to the photodetector and a gate connected to a snapshot signal;

a driver MOSFET having a drain connected to a row driver bus and a gate connected to a drain of the snapshot MOSFET;

a row driver circuit connected to the row driver bus;

an isolation MOSFET having a drain connected to a source of the driver MOSFET, a gate connected to an access signal, and a source connected to a column bus; and

a column buffer connected to the column bus;

wherein a tapered reset signal is applied to the reset MOSFET in order to reset the photodetector, and wherein during a reset operation, the row driver circuit grounds the driver transistor such that at least a portion of the column buffer acts as a current source for a feedback amplifier formed by the driver transistor, isolation transistor, and the column buffer.

21. The CMOS imager array circuit of Claim 20, wherein the row driver circuit and the column buffer are shared among a plurality of pixel circuits.